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ASIC Evaluator

Approved

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Executive Summary

This document describes the ASIC Evaluator, a 32-KNC node prototype built to demonstrate the EXTOLL ASIC technology and its use to realise the DEEP Architecture.

1 Introduction

During the official review of the DEEP project at month 24 (Jülich, 17.01.2014), the external reviewers strongly recommended the construction and installation of a prototype to test the EXTOLL ASIC network. This so-called "ASIC Evaluator" is to be installed at Jülich, where it will be connected to the existing DEEP Cluster.

At the official review at month 36 (16.01.2015) a preview of the "ASIC Evaluator" was shown in the DEEP server room. A smaller 3 node prototype system was used to show the external reviewers the proof of concept for the larger system.

The ASIC Evaluator (AE) will be used for software and application porting, with the objective of validating the "Tourmalet" technology and its use for the realisation of the DEEP concept [cite DEEP].

In addition to the existing DEEP System, the AE is a newly designed modular unit of 32 Booster Nodes. Each node consists of an Intel® Xeon Phi™ co-processor (referred to below as KNC) and an EXTOLL NIC. The NIC is realised with the EXTOLL ASIC Tourmalet PCIe board. The 32-node unit is packed in a 19 inch chassis with a height of 9 RU. The packaging is very dense and therefore the cooling must be done by a more efficient method than air flow or cold plates. This new type of chassis is named GreenICE (Green Immersion Cooled Electronics) and provides the densest packaging for high performance accelerators like the KNC with 250 W per chip by utilising immersion cooling with an inert fluid at a boiling temperature of 50 degree Celsius. It is the most efficient cooling method and thus environmentally compatible.

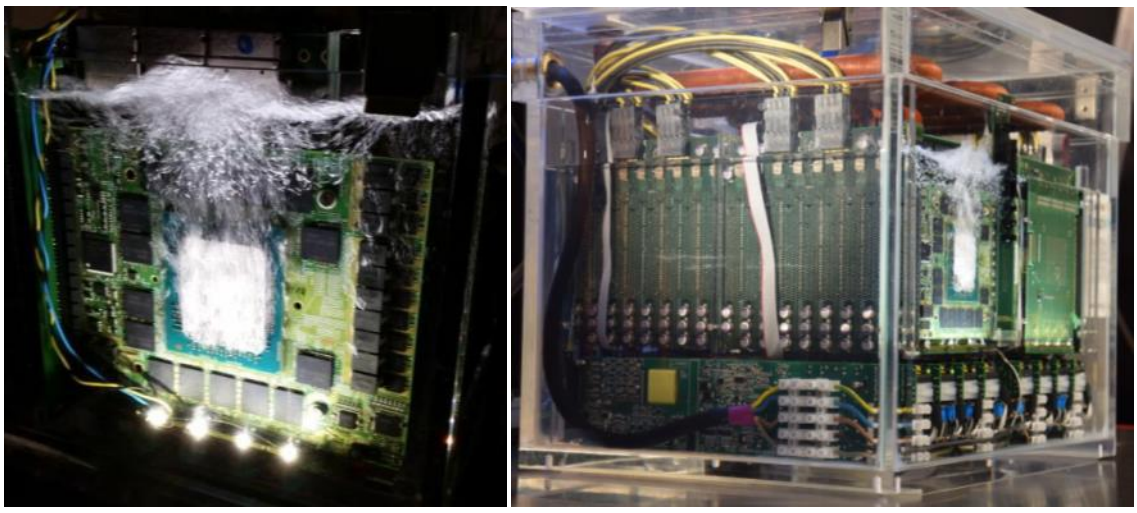

Figure 1: Prototype system (left), ASIC Evaluator (right).

This document lays out the technical description of that ASIC Evaluator.

2 Hardware architecture of the ASIC evaluator

The network topology of the AE is designed as a 3D torus of 32 nodes in a 4×4×2 torus logical arrangement. Four links of the Z-dimension are used to connect the AE to the two AE-BI nodes (BI: Booster Interface) within the rack to bridge between any Cluster interconnect and the EXTOLL interconnect in case of a heterogeneous network design. In a homogenous cluster which is completely build with the EXTOLL technology these Z-dimension links can be used to connect the AE-Booster nodes (AE-BN) directly with Cluster nodes making the BI superfluous. Within the DEEP Project the AE-BI nodes allow the AE to talk to the InfiniBand (IB) based Cluster part of the DEEP System.

In the following subsections the main functional components of the AE are described. Further technical specifications of the ASIC Evaluator and its components are given in the Annex (Section 6).

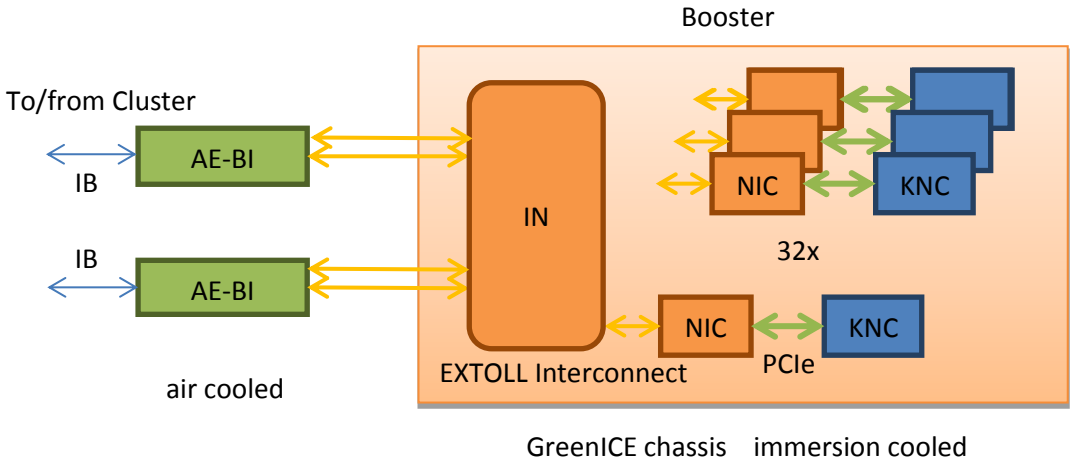

Figure 2: Block diagram of the ASIC evaluator.

Each KNC is connected via a PCI Express gen2 ×16 bus to the corresponding EXTOLL NIC. The NIC is configured as root port and thus can control the KNC for initialisation and booting without involvement of a PCIe connected server. These two components form one Booster Node of the AE. A Dense Backplane (DBP) is used to carry the PCI Express bus signals. One DBP can host 8 nodes with just a pitch of 18mm per node. Four DBPs are arranged in the chassis to host all 32 nodes of the GreenICE system. The peak performance of the chassis is about 1.2 TFlop/s ×32 = 38.4 TFlop/s.

The EXTOLL interconnect is realised by using electrical cables of various length in order to interconnect most of the nodes within the chassis. For a possible future optimisation step these links could be routed in a backplane.

The GreenICE prototype chassis is designed to demonstrate the high density of nodes in combination with the immersion cooling principle. It is mainly built with standard components with some small additional hardware, e.g. the dense backplane, in order to keep cost at a reasonable level and learn more about the specifics of immersion cooling.

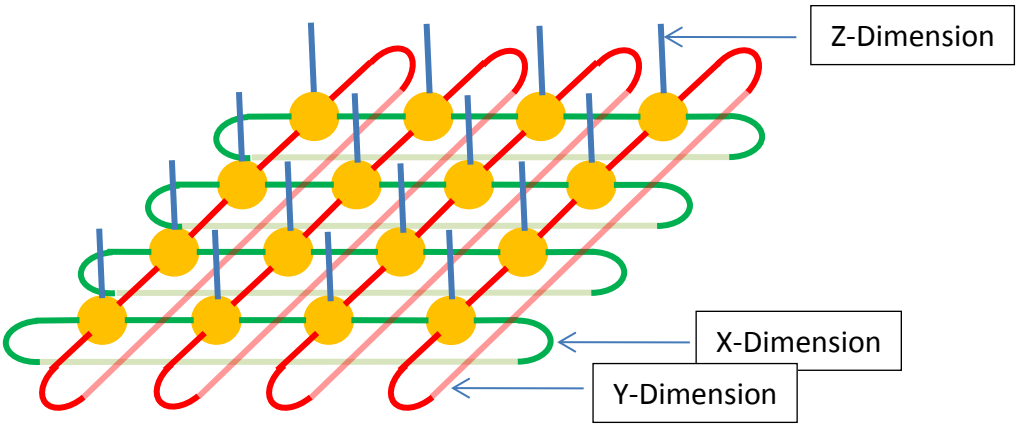

Figure 3: Lower layer of 3D Torus.

One layer of the EXTOLL interconnect structure is depicted in Figure 3 with just the X-Y dimension. The 4×4×2 structure is used only for the 32 node prototype chassis. In this case there is no need to close the torus in the Z-dimension because there is already one link between adjacent nodes.

The initial implementation of the ASIC Evaluator as shown at month 36 used as interconnect the A1 version of the EXTOLL ASIC, which provides 2.5 Gbit/sec/lane. The current A2 version of the EXTOLL ASIC has been tested and achieves a performance of 5 Gbit/sec/lane. At the time of this writing EXTOLL is working on a revision of the Torumalet PCB to achieve 8.3 Gbit/sec/lane. A future version of the GreenICE chassis will be built with this A2 revision "C" boards and this will further increase the performance of the AE.

The GreenICE chassis integrates all functional units required for the operation of the AE, which are the many-core nodes (KNC + NIC), the Power Supply Units (PSUs), the internal 3D torus cabling, the monitoring system including sensors as well as the cooling infrastructure. These parts are arranged in three levels, as depicted in Figure 4.

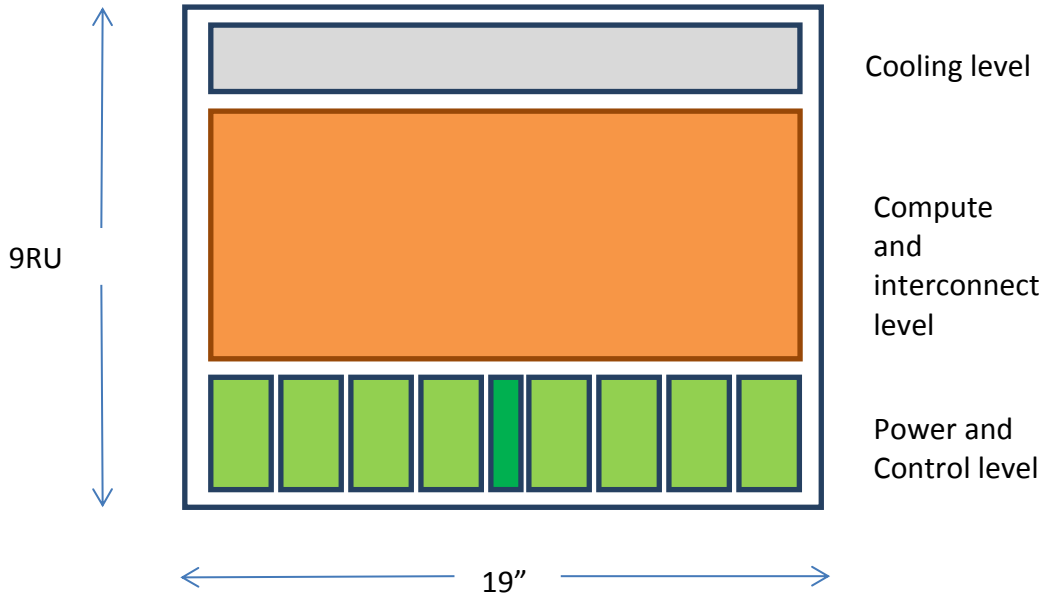

Figure 4: Levels of the GreenICE chassis.

2.1 Power and control level

The lowest level integrates eight server-type PSUs with 1200W each, and one control unit for the management of all components and the supervision of the immersion cooling process. The PSU-firmware has been modified to allow operation without fans. The metal enclosure and the fans are removed to improve heat transport and save space and weight. The heat dissipation of the PSUs provides some basic convection from the lower level and improves the heat transfer.

Figure 5: Power supply level showing 8 PSUs

2.2 Compute level

The second level contains the accelerator boards and the interconnect NICs. They are connected using a Dense Backplane (DBP) for the PCIe l×16 busses between each accelerator and the NIC. In order to keep cost at a reasonable level, mainly standard components are utilised, which are packaged in a dense way without the heat sinks typically needed when removing heat by air flow.

The DBP, as shown in Figure 6, can host Booster Node (one KNC and one NIC) in 18 mm pitch, leaving 7.4 mm space between boards, which is sufficient to allow immersion cooling of the components. All AE-Booster components are immerged in a basin filled with Novec 649, a cooling liquid from 3M [cite 3M]. Interconnect cabling is done on top of the “Compute and interconnect level” with optimised cable lengths, sharing some space with the cooling level. This shall not effect to overall concepts since the cables itself do not require any cooling.

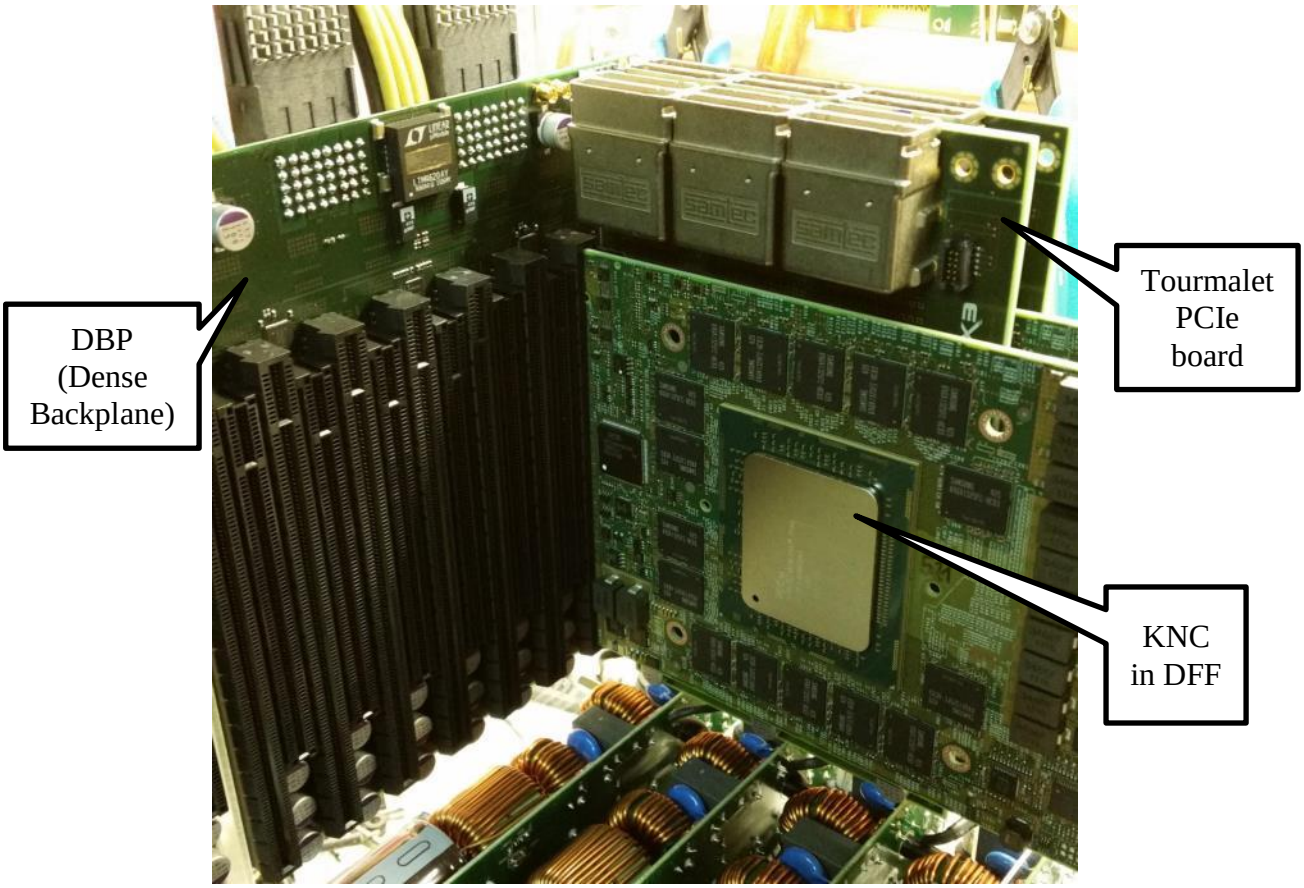

Figure 6: Dense Backplane with two KNCs and two EXTOLL NICs

2.3 Cooling level

The third level contains the infrastructure for the cooling of the Novec 649 fluid from 3M [cite 3M]. The fluid is not harmful to the environment, nontoxic, fully isolating, inflammable and compatible with the materials used for electronic components. Some care must be taken to avoid unwanted chemical reactions within the chassis, e.g. by cleaning of components from soldering flux.

A high performance copper pipe from Wieland AG is used to remove a maximum of 10 kW of power dissipation from the chassis. The pipes are designed such that they are 4-5 times more efficient than standard copper pipes [cite Wieland]. In addition to the external surface they have an internal structure to break up the laminar flow of water and thus to improve the heat transfer from the pipe wall to the liquid cooling media (here: water).

Figure 7: Copper pipe structure in cooling level

The advantages of immersion cooling are manifold. The most important feature is the very efficient heat removal from the high power components by using the phase change of Novec at the specific boiling temperature of 50°C. This allows for packaging the electronic components in an extremely dense way. The generated vapour creates a fluid flow which cools all other components just by vapour-driven convection. This renders obsolete pumping of fluid within the chassis. The vapour rises up to the cooling level where it is condensed back to fluid by the copper pipe, through which cooling water is circulating. All components are operated at the same constant temperature which avoids overheating of some critical areas and increases lifetime of components.

Using a throughput-controlled water flow through the copper pipe, an outlet temperature of 50°C can be achieved and thus warm water cooling can be used. The inlet temperature can be as high as 35°C leaving a 15 °C temperature difference for cooling. This allows operating an external chiller at environmental free-air conditions without any fan or water spraying, making the GreenICE chassis extremely energy efficient.

The chassis is a closed system, where neither vapour nor fluid can be lost. In the initial heating phase a small amount of pressure is generated which is compensated by a small expansion tank. The small operating pressure is measured and included in the monitoring and control environment.

It should be mentioned that there are also some disadvantages of immersion cooling: Most important is the closed chassis system, where access to the internal components is restricted to a completely powered down and cooled down chassis for maintenance. Therefore, the chassis is constructed in a way that it can be removed easily from a rack for maintenance. A second one is that all cable vias through the chassis must be built in a gas-tight manner to avoid losing fluid or vapour over operation time. Minimising the number of external connections was one of the goals of the prototype design.

There are only three types of connections.

- First, there is the power cord to supply the 3×240V three phase power to the chassis. It is internally distributed to the PSUs in a balanced way. The power cord plugs into the rack supply with a CEE connector.
- The second type of connections are the network links with their interconnect cables, which can connect the AE to a host system. The amount of cabling here is dependent on the system architecture. For large scalable systems a different wiring scheme must be designed in order to provide all surface links of a 3D torus from one chassis to the neighbouring ones. In the 32-node prototype GreenICE this would require 32 links in the Z dimension and some more in the X and Y dimensions, which depends on the torus configuration. The 4×4×2 torus would require 2×2×4 + 2×2×4 + 2× 4×4 = 64 links for full expandability.
- The third connection is the water pipe for the cooling loop. It uses flex pipes for the connection to the rack mounted distribution pipes and water stop valves to simplify disconnecting. Inside the chassis this pipe is fully sealed to avoid any leakage of water.

The GreenICE chassis is a modular and easy to install unit for 32 nodes.

3 GreenICE chassis management

The GreenICE chassis is controlled by a management processor, independent of all other electronics. It is powered by a separate standby power supply. The GreenICE chassis is supervised by this stand-alone Linux Raspberry Pi [cite RASPBERRY] system with measurement extensions, which allows controlling and monitoring the internal status of the immersion cooling chassis.

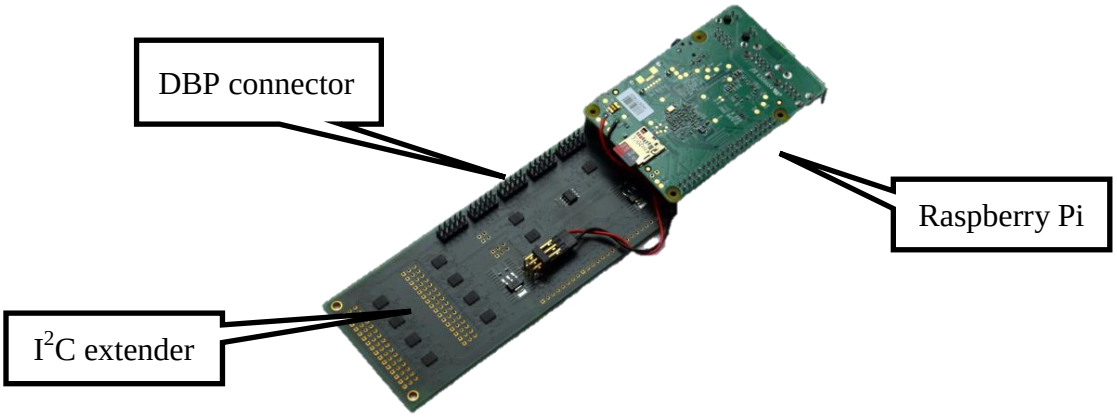

Figure 8: GreenICE management controller.

This controller is remotely accessible via Ethernet and ssh. It performs all measurements in order to supervise the chassis and takes protection measures in case of emergency, such as shut down of KNCs, PSU switch off, etc., without the need of external human or environmental intervention. Furthermore, it can access the I^2C debug interface of the Tourmalet ASIC and thus read out all internal registers for debugging and control operations. In addition, the Tourmalet itself has an I^2C connection to the KNC through the DBP. This allows for accessing even the internal register file of the KNC. These I^2C interconnections build a slow control network which gives access to all internal register files and sensor chips within the chassis independent of the EXTOLL interconnect. All these control and status registers can also be accessed in a high performance mode by using the EXTOLL interconnect when the system is in normal operation mode.

Additionally, all sensor information is provided to an external management server. Data read out is performed through Ethernet access.

4 Current status and next steps

The immersion cooling principle has been tested with a small test system of 3 DFF KNCs and three EXTOLL NICs. The GreenICE chassis for 32 KNCs is completed with all mechanical and electronic components. Some delay has been encountered during the bring up of the ASIC Evaluator. The following sections describe the issues in more detail.

4.1 Temperature

As part of the system tests, the 3 node prototype system was subject of thermal tests. These tests took place in the smaller system due to delay in the delivery of the A2 ASIC and ongoing construction work of the GreenICE chassis.

Contrary to the assumption, that a fluid with a boiling point of 5 ^oC keeps all components at a temperature below this point a KNC die temperature between 110-120 ^oC was measured. We discussed this together with experts of Intel and 3M and came up with different solutions. 3M proposed to attach a boiling enhancement coating (BEC) on the head spreader of the KNC.

This BEC is a thin cupper plate with a very rough surface texture and drastically increases the heat transfer between the heat spreader and Novec 649. This would be the most efficient approach in reducing the die temperature, but due to manufacturing difficulties this is not possible to realise.

Intel's recommendation was to seal the hole in the heat spreader with silicone to avoid Novec649 fluid to enter the cavern between the heat spreader and the KNC's chip package. Fluid in this cavern would vaporize during the operation of the KNC, becomes an isolator and decreases the heat transfer. After sealing the hole the die temperature during the thermal tests was reduced to 80-90 ^{o}C. This is a comparable temperature with the air-cooled operation of the KNCs and the cooling in the Booster chassis.

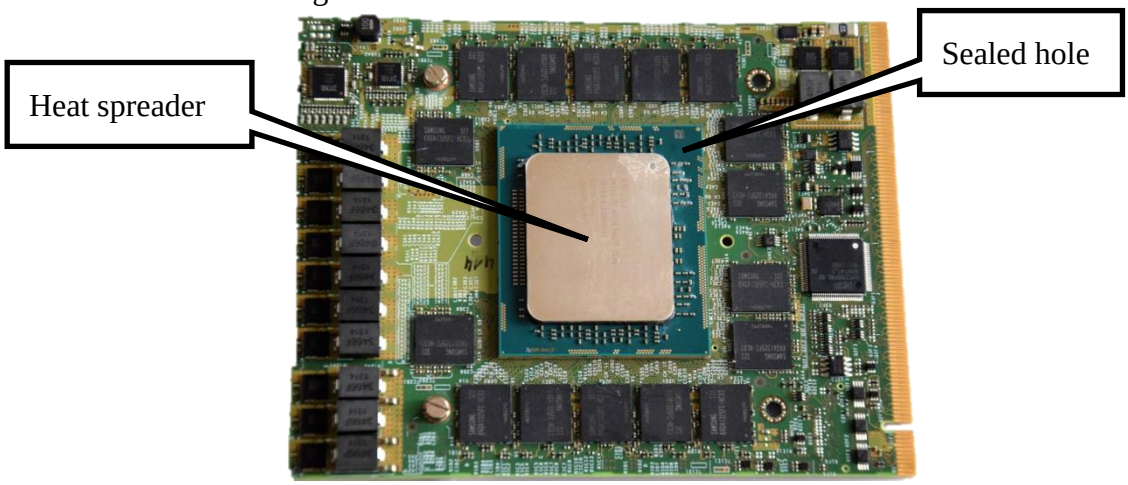

Figure 9: Dense form factor KNC with sealed hole.

4.2 Reference clock and power distribution

The biggest delay in the delivery of the ASIC Evaluator to Jülich was caused by electromagnetic interference on the DBP, which was discovered very late in the validation process. The lab environment at UniHD is not equipped for liquid cooling and has not the infrastructure to cool a system which dissipates 12KW of heat. Nevertheless, to test the components in the ASIC Evaluator prior to the delivery, all tests were limited to 4 nodes on a single DBP which could be handled by the chiller available in the lab. During the tests failing PCIe links were discovered between the Tourmalet and the KNC cards. The measurement based determination proves to be difficult, because all measurements had to take place in the fluid filled GreenICE chassis to operate the nodes and also the limited available space inside the GreenICE chassis represented a particular challenge. A lot of time and effort was spent to add probes to various components of the DBP to get insight why the PCIe link could not be trained. I turned out, that above a certain load the DC/DC switching converter on the DBP introduced peaks into the power planes which affected the clock buffers. These disturbed the distribution of a PCIe reference clock to the Tourmalet and KNC cards. The short-term workaround can be seen on Figure 10. The converter on the DPB is now disabled and the DC/DC conversion from 12V to 3.3V is now done on separate board. At the time of this writing the described fix was successfully implemented for one DBP and is ongoing for the remaining DBPs.

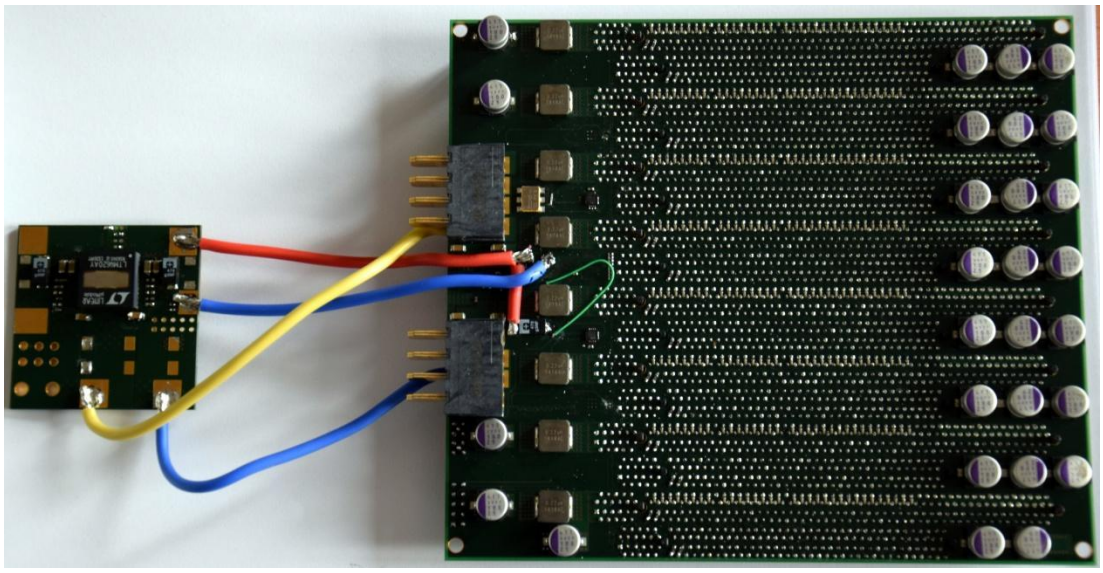

Figure 10: DBP and 12V to 3.3V DC/DC converter on additional board

4.3 Installation at Jülich

The installation of the ASIC Evaluator at the Jülich Supercomuting Centre is not yet done due to the ongoing work on fixing the problem described in section 5.2. The delivery is planned for the beginning of July. The preparations done in the local infrastructure for the installation of the ASIC Evaluator are described in Deliverable D6.5, submitted at the same time as the present document.

5 Acknowledgements

We want to thank all contributing companies (Wieland, 3M, Intel) for their support and help in making GreenICE a working prototype of immersion cooled electronics. Furthermore we want to thank Megware Computer GmbH for the system integration of the AE-BI and the rack infrastructure for the GreenICE chassis.

6 Annex: Technical specifications of ASIC Evaluator

The following sections show the technical details of the various components of the ASIC Evaluator.

Component	Amount
Intel Xeon Phi = KNC (7120D)	32
EXTOLL ASIC PCIe cards (“Tourmalet” A2).	32
Cables (internal for 3D torus)	80
Power supply (server PSUs with 1200W each)	8
Dense Backplane (each DBP can host 8 KNCs and 8 EXTOLL PCIe boards	4
AE-BI Servers	2
Chassis	1
Rack	1
Cooling fluid (immersion cooling of AE-Booster) 3M Novec 649	20 liter
Chassis monitoring unit (RaspberryPi with multiple SMBus extensions)	1

6.1 Intel Xeon Phi (KNC)

Model	7120D Dense Form Factor (DFF) version, 61 cores
Amount	32
Function:	AE-Booster Node functionality: computation
Communication	KNC PCIe to/from EXTOLL PCIe with gen2 (max. 10GB/s)
Comments	Peak DP FP performance of 1.2TFLOPS

6.2 Tourmalet (EXTOLL ASIC in PCIe card)

Amount	34
Function:	32 cards for Interconnect between AE-Booster Nodes 2 cards for communication with the DEEP Cluster (BI functionality)
Communication	PCIe to/from KNC PCIe, 6 links for 3D Torus IN, 7th link unused

6.3 Dense Backplane (DBP)

Amount	4
Function:	PCIe Connection between KNC and EXTOLL NIC
Communication	8 local PCIe connections
Management functions	Supply of PCIe ref clock signals and 12V + 3.3V power supply and filtering. Control of PCIe reset signals, connection of SMBus from EXTOLL to KNC for management functions
Comments	This DBP is used to build 8 BN nodes by connecting 8 KNCs with 8 EXTOLL NICs.
	Packaging of 8 BNs used just for modular optimisation

6.4 Server (AE-BI)

Amount	2 (named BI in the DEEP concept)
Function:	Remote boot of KNCs and bridge between EXTOLL network (in the AE) and InfiniBand network (in the

	DEEP Cluster), BI function
HD	500GB SATA
Communication	IB / Tourmalet-EXTOLL / Eth
InfiniBand HCA	FDR, Mellanox ConnectX3, supports QSFP connectors
Comments	Supermicro Server board: X9DRT-IBFF

6.5 Cables

Amount	80 electrical
Function:	2×16 Xdim, 2×16 Ydim, 1×16 Zdim 4×4×2 3D Torus
Communication	80 ×12 links for 3D-Torus interconnect
Comments	2 Infiniband QSFP cables: connection from AE-BI servers to Cluster

6.6 Mechanics

Number of chassis/rack	1
Max. power dissipation per GreenICE chassis (delivery, cooling)	12KW
PSU redundancy per chassis	no
Number of AE-BI servers/ chassis	2
Max. power dissipation per server (delivery, cooling)	1 KW
Number of racks	1
Cooling: - water cooling for GreenICE inlet temperature up to 35^{o} C, - air cooling for AE-BI server chassis	

The AE include all components required for signalling, power supply and cooling (e.g. signalling backplane, water manifolds, power distribution) to operate the 32-node GreenICE chassis.

6.7 AE network

EXTOLL implementation	Tourmalet ASIC
Minimum internal link bandwidth	1 GByte/s
Minimum raw link bandwidth Tourmalet version A2	5 GB/s
Lane count per link	12
Physical link layer bit error rate	*<1E-12*
PCI-Express interface to KNC/BI host	×16, Gen2
Torus Topology	4×4×2

6.8 AE-Cluster network

Link speed and type	FDR IB

6.9 Safety

Overcurrent protection (Fuse@each power supply of 1200W)	Per KNC/EXTOLL node group of 4
Leakage sensors	Per chassis
Temperature sensors	Per node

6.10 Reliability/Maintenance

Expected lifetime	1 year
Application visible transient MTBF excluding KNC	>7 days
Permanent failure MTBF excluding KNC	30 days
Number of permanently failed AE-BIs tolerated in operation	1
Number of permanently failed AE-BNCs tolerated in operation	5
Availability (per year)	95%
In operation swap of AE-BNC and AE-BI modules (hot plugging)	No
Scheduled maintenance interval	3 months
Scheduled maintenance downtime (excluded from availability)	1 day

To meet the availability targets a respective inventory stock of critical components (e.g. AE-BNC, AE-BI, IB network cards, PSU) is kept. Minimum required items are:

Tourmalet cards	3
Server	1
KNCs	2

6.11 Documentation

For operation of the ASIC Evaluator documentation is available, which describes the various procedures for operation and maintenance. Initial versions of the documents will be available at delivery time and will be updated as soon as new procedures are defined.

- Instructions for regular power up and power down procedures.
- Instructions for filling, monitoring and maintaining the liquid cooling system, including composition of cooling liquid, coolant test procedures, coolant exchange interval and procedures.
- Instructions to be followed in case of unforeseen shutdowns, system excursions and emergencies.

References and Applicable Documents

[cite DEEP] http://www.deep-project.eu/deep-project/EN/Home/home_node.html

[cite 3M] http://solutions.3m.com/wps/portal/3M/en_US/3MNovec/Home/ProductCatalog/?PC_Z7_RJH9U5230OOA50IEKHCMDN11H0000000_nid=F55Z1XTKWXbeQQBXSJ1LVVgl

[cite Wieland] http://www.wieland-thermalsolutions.de/internet/de/products/finned_tubes/hochleistungsrohre/Hochleistungsrohre.jsp

[cite EXTOLL] http://www.EXTOLL.de/index.php/productsoverview/green-ice

[cite RASPBERRY] http://www.raspberrypi.org/

List of Acronyms and Abbreviations

A

AC/DC: Alternating Current / Direct Current
AE: ASIC Evaluator: prototype to test the use of the EXTOLL ASIC technology for the DEEP concept.
AE-BN: Booster Node of the ASIC Evaluator, constituted by one KNC and one EXTOLL Tourmalet (PCIe-) card.
AE-rack: Rack of the ASIC Evaluator.
ADC: Analog Digital Converter
API: Application Programming Interface
ASHRAE: American Society of Heating, Refrigerating and Air-Conditioning Engineers
ASIC: Application Specific Integrated Circuit: Integrated circuit customized for a particular use
ATOLL: Predecessor of EXTOLL

B

BI: Booster Interface (functional entity)
BMC: Baseboard Management Controller
BN: Booster Node (functional entity)
BoP: Board of Partners for the DEEP project
BSCW: Basic Support for Cooperative Work: Software package developed by the Fraunhofer Society, used to create a collaborative workspace for collaboration over the web

C

CEE: International standard used for cables and other components.
CN: Cluster Node (functional entity)
Coordinator: The contractual partner of the European Commission (EC) in the project
CPU: Central Processing Unit

D

DBP: Dense Backplane: backplane of the ASIC Evaluator, supporting 8 AE-BNs
DC: Direct Current (electricity)
DDG: Design and Developer Group of the DEEP project
DEEP: Dynamical Exascale Entry Platform: EU-FP7 Exascale Project led by Forschungszentrum Juelich
DEEP Architecture: Functional architecture of DEEP (e.g. concept of an integrated Cluster Booster Architecture)
DEEP Booster: Booster part of the DEEP System
DEEP System: Prototype built within the DEEP project as a combination of Cluster and Booster
DFF: Dense Form Factor
DMA: Direct Memory Access
DoW: Description of Work: Annex I of the Grant Agreement

E

EC: European Commission
EU: European Union
Eurotech: Eurotech S.p.A., Amaro, Italy

Exaflop: 10^{18} floating point operations per second
Exascale: Computer systems or applications, which are able to run with a performance above 10^{18} floating point operations per second
EXTOLL: High speed interconnect technology for cluster computers developed by University of Heidelberg
EXTOLL evaluator: Platform for evaluation of EXTOLL technology, developed and used in the DEEP project

F

FDR: Fourteen Data Rate: Communication signalling technique of InfiniBand
FLOP: Floating point Operation
FPGA: Field-Programmable Gate Array: Integrated circuit to be configured by the customer or designer after manufacturing

G

GB: Giga Byte
Gb: Giga Bit
Gb/s: Giga Bit Per Second
GFlop/s: Gigaflop, 10^{12} floating point operations per second

H

HCA: Host Channel Adapter
HPC: High Performance Computing
HW: Hardware

I

I²C / I2C: Inter-Integrated Circuit. Serial computer bus used for attaching low-speed peripherals to computer motherboards and embedded systems
IA: Intel Architecture
IB: InfiniBand
ICT: Information and Communication Technologies
IEEE: Institute of Electrical and Electronics Engineers
Intel: Intel GmbH Braunschweig, Germany
Intel Xeon® Phi™: Official product name of the Intel Many Core (MIC) architecture processors. The first available Intel Xeon® Phi™ product is code-named Knights Corner (KNC).
I/O: Input/Output
IP: Intellectual Property or Internet Protocol (depending on the context)
IT: Information Technology

J

JSC: Juelich Supercomputing Centre
JUELICH: Forschungszentrum Jülich GmbH, Jülich, Germany

K

KB: Kilo Bytes
KNC: Knights Corner: Code name of a processor based on the MIC architecture. The commercial name of this product is Intel Xeon® Phi™.
KNF: Knights Ferry: Intel first available processor based on the MIC

L

Linux: A Unix-like computer operating system assembled under the model of free and open source software development and distribution

M

MB: Mega Byte or Mother Board (depending on the context)
MIC: Intel Many Integrated Core architecture
MIC-OS: Operating System of the MIC architecture

N

NIC: Network Interface Card: Hardware component that connects a computer to a computer network

O

OS: Operating System

P

PCB: Printed Circuit Board: Board used in electronic to mechanically support and electrically connect electronic components
PCI: Peripheral Component Interconnect: Computer bus for attaching hardware devices in a computer
PCIe: PCI Express: Standard for peripheral interconnect, developed to replace the old standards PCI, improving their performance
PFlop/s: Petaflop, 10^{15} floating point operations per second
PM: Person Month or Project Manager of the DEEP project (depending on the context)
PMT: Project Management Team of the DEEP project
PSU: Power Supply Unit

Q

QDR: Quad Data Rate: Communication signalling technique of InfiniBand

R

R&D: Research and Development
RTD: Research and Technological Development

S

SATA: Serial Advanced Technology Attachment: Computer bus interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives

SMFU: Shared Memory Functional Unit
SW: Software

T

TFlop/s: Teraflop, 10^{12} floating point operations per second

U

UniHD: University of Heidelberg, Germany

V

W

WP: Work Package

X

Y

Z