DEEP

Dynamical Exascale Entry Platform

Grant Agreement Number: 287530

D1.4
Midterm management report at month 18

Approved

Version: 2.0
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Date: 24.02.2014
**Project and Deliverable Information Sheet**

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<tr>
<th>DEEP Project</th>
<th><strong>Project Ref. №:</strong> 287530</th>
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<tr>
<td><strong>Project Title:</strong> Dynamical Exascale Entry Platform</td>
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<td><strong>Project Web Site:</strong> <a href="http://www.deep-project.eu">http://www.deep-project.eu</a></td>
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<td><strong>Deliverable ID:</strong> D1.4</td>
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<td><strong>Deliverable Nature:</strong> Report</td>
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<tr>
<td><strong>Deliverable Level:</strong> CO *</td>
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<tr>
<td><strong>Contractual Date of Delivery:</strong> 31 / May / 2013</td>
<td></td>
</tr>
<tr>
<td><strong>Actual Date of Delivery:</strong> 31 / May / 2013</td>
<td></td>
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<tr>
<td><strong>EC Project Officer:</strong> Luis Carlos Busquets Pérez</td>
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**Document Control Sheet**

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<td><strong>Version:</strong> 2.0</td>
<td><strong>Status:</strong> Approved</td>
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<td><strong>Software Tool:</strong> Microsoft Word</td>
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<td><strong>File(s):</strong> DEEP_D1.4_Midterm_management_report_at_M18_v2.0-ECapproved-PublishablePart.docx</td>
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# Document Status Sheet

<table>
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<th>Version</th>
<th>Date</th>
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<th>Comments</th>
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<tr>
<td>1.0</td>
<td>31/May/2013</td>
<td>Final</td>
<td>Submitted to EC</td>
</tr>
<tr>
<td>2.0</td>
<td>24/February/2014</td>
<td>Approved</td>
<td>Approved by EC</td>
</tr>
</tbody>
</table>
Document Keywords

| Keywords:               | DEEP, HPC, Exascale, status report, month 18 |

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Executive Summary

The Dynamical Exascale Entry Platform (DEEP) project started on 1st December 2011 and will last three years. The main goal of the project is to develop a prototype hardware and software supercomputing system with the potential to reach a peak performance of 100 PFlop/s in 2014, paving the way towards Exascale systems by the end of the decade. DEEP will optimise a set of grand-challenge applications with high societal impact and generic algorithmic structure for this platform. The key innovation of the DEEP project is its holistic Exascale-enabling concept integrating the architectural, system software and application level. The strategic goals of DEEP are (i) to contribute to an independent provision of general purpose Exascale performance supercomputers for the European HPC research infrastructure PRACE, (ii) to advance the growth of ICT and HPC hardware and software technology developed and produced in Europe, and (iii) to expand worldwide leadership and competitiveness of Europe’s computational scientists and engineers.

This report describes the objectives, work performed, resources used, and results achieved during months 13 to 18 of the DEEP project. The main achievements in the reporting period are enumerated below:

- Second review (at month 12) successfully passed.
- Preparation of an amendment of the DoW to include two Third Parties in the consortium, adaptation of the working schedule, and the prolongation of the project
- Installation of the DEEP Cluster at Juelich completed with the connection of its InfiniBand network.
- Progress in the definition of the functionality to be implemented in the RAS plane to measure the energy consumption of the final DEEP system.
- Progress in the DEEP Booster design: design of BIC (based on EXTOLL’s FPGA version) almost finished; BNC board (based on Intel Xeon® Phi™ in PCIe form factor and on EXTOLL FPGA) tests on-going.
- Tests and first improvements in the implementation of the low-level Cluster-Booster protocol.
- Extension of the ParaStation component pscom to support EXTOLL completed.
- Extension of the OmpSs offloading functionality to support both C and Fortran codes. Tests with applications from WP8 on-going.
- Application improvements in performance and porting to the MIC evaluator (Intel Xeon® Phi™ cards) on-going.
- Presentation of DEEP in publications, workshops and conferences.
- Organisation of a joint DEEP/Mont-Blanc workshop for technical discussions on common topics.
1 Publishable summary

Numerous challenges must be overcome to reach Exascale by the end of the decade. When starting from current PFlop systems a factor of 1000 in performance increase is required. Investigating the roadmaps of standard CPUs reveals that it will not be sufficient to update and scale the concept of current cluster systems. In order to meet the requirements of energy-efficiency the use of accelerators becomes inevitable. However, today’s solution of accelerated clusters –i.e. cluster with accelerators attached to each node– will not carry us to Exascale. On the one hand this is due to the inflexibility originating from the static assignment of standard CPUs and accelerators; on the other hand the competing use of the system bus by both accelerator and interconnect, combined with the lack of ability of the accelerator to use the interconnect autonomously, seriously limits the scalability of this solution.

Therefore, the DEEP Architecture proposes to detach the accelerators from the standard CPUs and to gather them into a separate cluster of accelerators that is called Booster. It is foreseen to run the highly scalable parts of the applications on this part of the DEEP System. The Booster is connected to a standard Cluster qualified to handle those parts of an application not suited for the Booster. The benefits are manifold: there is more flexibility on the ratio of standard CPUs and accelerators to be used by an application, the ability of the accelerators in the Booster to act autonomously allows for off-loading more complex and more parallel kernels, and an extended programming-model will support the application-developers in the identification of these offload-kernels and in porting their workload to the proposed architecture.

1.1 Project objectives

The specific objectives of the DEEP project and first results are:

- Development of a prototype hardware platform consisting of a Cluster element based on multi-core chips, a Booster element based on many-core technology and a commensurate connectivity, following the components-off-the-shelf philosophy. This prototype of Cluster Booster Architecture will serve as proof-of-concept for a next-generation PRACE production system reaching up to 100 PFlop/s in the time-frame 2014/2015, with the potential to achieve Exascale between 2018 and 2020.
  \(\Rightarrow\) Cluster part installation in Jülich completed.
  \(\Rightarrow\) Prototypes of several Booster components are being tested.
- Combination of innovative technologies for the Booster element: novel Intel many-core processors; EXTOLL high speed interconnect; hot water cooling.
  \(\Rightarrow\) First prototypes of Booster Node Card (BNC) are being tested at Eurotech. One BNC contains two nodes, each with an Intel Xeon\textsuperscript{®} Phi\textsuperscript{TM} and an EXTOLL FPGA to implement the network.
- Development of a reliable, open source cluster operating system, interconnect and runtime software stack with high resilience while exploiting millions of cores.
  \(\Rightarrow\) Software environment and programming model for DEEP have been defined.
  \(\Rightarrow\) Optimisation of the Cluster Booster Protocol on-going.
  \(\Rightarrow\) Cluster Booster Protocol plugin in ParaStation \textit{pscom} implemented.
  \(\Rightarrow\) ParaStation component \textit{pscom} supporting EXTOLL (D4.3).
→ OmpSs runtime (Nanos++) ported to Intel Xeon® Phi™.
→ OmpSs offloading mechanism supports now both C and Fortran codes.

- Development of programming models, scientific libraries and performance tools for standard x86-based many-core processors, in order to achieve high productivity and enabling unprecedented scalability.
  → First performance measurements of Intel MKL BLAS library routines have taken place.
  → The application codes to determine the libraries used and their parameters have been analysed in detail.
  → Paraver/EXTRAE performance tool ported to MIC.
  → Scalasca performance tool ported to MIC.

- Improvement of current cluster energy efficiency by an order of magnitude exploiting novel many-core chip technologies and advanced software-aided cooling technologies with a power usage effectiveness approaching a value of 1.
  → Hot water cooling infrastructure prepared and operating in Juelich.
  → Concepts for improving energy and cooling efficiency defined.
  → Functionality needed on the RAS plane defined. Implementation on-going.

- Optimisation of a set of application codes on the DEEP System that are representative for future Exascale computing and data handling requirements, chosen from the fields of Health and Biology, Climatology, Seismic Imaging, Computational Engineering, Space Weather, and Superconductivity and proving safe extrapolation to millions of cores as will be required with future Exascale systems.
  → Structure of the applications has been analysed and initial strategies to distribute the codes between Cluster and Booster has been identified.
  → Optimisations of the codes and porting to MIC are on-going.

- Demonstration of scalability of the new hardware-software concept with respect to the generic multi-scale, adaptive grid and long-range force parallelisation models underlying the application codes.
  → Demonstration will be first possible when the complete system is available.

- Dissemination of the innovations and results of the project to the public.
  → The DEEP project and its first results have been presented in multiple meeting, conferences, and workshops. Details are given in the list of dissemination activities provided in Annex A.1 of this report.

### 1.2 Work performed and main results

With the installation of the InfiniBand network at the beginning of 2013 the DEEP project has achieved milestone MS17: “Installation of the Cluster Subsystem completed”). Milestone number 3 was achieved in January 18th 2013 with the successful completion of the second project review.

**Management, legal and administrative tasks**

In the present reporting period the management activities focused on monitoring the progress of the project to guarantee the achievement of all technical goals specified in the Description of Work (DoW) and the fulfilment of all commitments to the European Commission, including the preparation of the second external review.
The Management team organised the agenda for the second review meeting (at month 12) which took place on the 18th January 2013 in Mannheim (Germany). To fulfil the internal quality policies a rehearsal meeting one day before the review was conducted. As a result of the second review, the project has been evaluated as doing “good progress”. Additionally, all deliverables submitted in the first year of the project were approved.

Following the recommendations from the review, the DEEP project has prepared an amendment of the Description of Work (DoW) to adapt the work-plan to the hardware availability and include two Third Parties in the consortium. The official request for the amendment will be sent to the Project’s officer end of May. Following that, the DoW will be updated on the NEF server.

Monthly teleconferences of the Team of Work Package leaders (ToW) were organised to periodically discuss the progress in all Work Packages (WPs). The fourth regular face-to-face meeting of the consortium (BoP) took place in Bologna (Italy) on the 15th – 16th May 2013. Here, the status of the project was discussed with particular emphasis on the amendment of the Description of Work. The proposed amendment was approved by the Board of Partners. All Deliverables were timely submitted to the European Commission after having passed through the mandatory DEEP internal review process.

**Dissemination, training and outreach**

The centre of the dissemination activities of DEEP is its web site: [www.deep-project.eu](http://www.deep-project.eu). The DEEP web page has been updated in the reporting period to keep track with the project results (i.e. with presentations, publications, and approved public deliverables) and to announce all upcoming events.

Partners from the DEEP consortium presented the project’s concept in several conferences and workshops, such as the 2nd IS-ENES Workshop on High performance computing for climate models in Toulouse (France), or the Exascale Applications and Software Conference in Edinburgh (UK). Three papers showing DEEP results were accepted at the latter conference, and are currently under preparation (deadline 1st July 2013). A joint BoF session together with Mont-Blanc and CRESTA has been submitted and accepted by the ISC’13 organisers (BoF no.1, scheduled on Tuesday 18th June 2013 at 9:00). An updated flyer explaining the goals and most important aspects of the DEEP project will be distributed at ISC’13.

Training the community on how to use the software and hardware developed in DEEP is an important part of the project. The main goal of the training events in DEEP is to teach the application developers participating in the project on how to use the software tools and programming environment running on the DEEP System and other intermediate prototypes. The third Mont-Blanc/DEEP Training Workshop took place from the 11th to the 13th March 2013 in Barcelona (Spain). An intensive course including lectures and numerous hands-on sessions on OpenCL and OmpSs programming with special focus on its support for Fortran, was offered to all members of the DEEP and Mont-Blanc projects.

Coupled with the previously mentioned training event a workshop to strengthen the collaboration between the EU Exascale Projects DEEP and Mont-Blanc was held in Barcelona on 14th March 2013. This one-day meeting allowed for an open technical discussion on various aspects of the two projects, including their hardware architectures, software environment, and applications work. Common topics were discussed and a rich
interchange of experiences took place. The discussion was highly appreciated by members of both projects.

Following the success of the event, a new workshop, this time with the three Exascale Projects CRESTA, DEEP, and Mont-Blanc is planned for 10th-11th June 2013 in Barcelona, focusing on software environment, performance analysis tools, and applications.

All dissemination and training activities performed in the present reporting period are enumerated in Annex A.1 of this report.

**Technical Work**

The technical work in DEEP is grouped into the three main parts: system hardware, system software, and applications.

In the hardware concept of DEEP (see Figure 1) a standard Cluster, composed of multi-core processors and the high flexibility network InfiniBand®, is attached to a Booster of Intel Xeon® Phi™ processors connected via a highly scalable EXTOLL torus network.

![Figure 1: Sketch of DEEP hardware architecture (CN: Cluster Node; BN: Booster Node; BI: Booster Interface)](image)

The DEEP software stack (see Figure 2) focuses on scalability and an efficient use of resources. The parts of the application with a complex communication pattern (low to medium scalability) will run on the DEEP Cluster, while the code parts with regular communication patterns (highly scalable) will run on the Booster. The DEEP programming environment provides a Global MPI layer below the OmpSs (BSC) tasking model to help the developers in decomposing their applications into tasks in order to efficiently overlap the use of the Cluster and the Booster sides.
D1.4

Midterm management report at month 18

System Hardware

On the hardware side the work within the reporting period on the construction and test of the various elements of the DEEP Booster has progressed. The first version of Booster Node Card (BNC), based on a standard PCI Express form factor Intel Xeon® Phi™ and an Altera Stratix V FPGA running EXTOLL, is currently in its bring-up phase (see Figure 3). The flow of electrical signals through the board and its mini-backplane has been verified and the port of EXTOLL to Stratix V is expected to finish by the end of May. Once it is available, the boot process of the Intel Xeon® Phi™ cards through EXTOLL will be tested and the verification phase of the BNC board will finish. The BIC is being developed in parallel.

Once both prototypes of BIC and BNC boards are tested, they will be assembled on the Proto-Booster, a small-sized Booster prototype on EXTOLL-FPGA and Intel Xeon® Phi™ in PCIe form factor which will be used for software development until the EXTOLL-ASIC is available. The Proto-Booster will be integrated in a self-cooling rack. First samples of this kind of rack are already available at Eurotech and will be tested in the coming weeks.
In the present reporting period the installation of the DEEP Cluster was completed with the integration of its InfiniBand network. Operating system, file system and a general software environment were previously available and have been frequently updated. Several stability and stress tests have been used to verify the correct functioning of all hardware and software the elements of the system. An optimised LINPACK run is planned for the coming weeks. The DEEP Cluster, its environment and the login and file system servers are part of the in-kind contribution to the project by JUELICH.

The MIC evaluator has been upgraded substituting its KNF by KNC\(^1\) cards. Currently it is constituted by two workstations, each equipped with two KNC cards. Its configuration has been updated to allow for running MPI programs on all cards and nodes. The MIC evaluator is being used for software development and application porting.

System Software

On the software side, the implementation and porting of the various elements involved in the DEEP software stack have progressed in the present reporting period according to plan. The implementation of extensions on the MIC-OS to support EXTOLL communication and the port of EXTOLL to MIC are on-going. The Cluster Booster Protocol has been further tested, debugged and refined and, based on it, a plugin for ParaStation pscom has been implemented. The first prototype of the Booster resource management with dynamic allocation in Torque and Maui is already available. ParaStation MPI has been extended to support EXTOLL (documented in D4.3). The realisation of Global MPI has progressed with the implementation of MPI\_Comm\_connect and the parts of MPI\_Comm\_spawn responsible for communication and process management.

The work on the OmpSs programming environment has also progressed: the Nanos++ execution runtime and the Extrae instrumentation library have been ported to the Intel Xeon\textsuperscript{\textregistered} Phi\textsuperscript{TM}. The Scalasca measurement system has also been ported to the Intel Xeon\textsuperscript{\textregistered} Phi\textsuperscript{TM}. Nanos++ and the Mercurium compiler have been extended to support the MPI offloading directives for both C and Fortran. WP8 applications written on C and Fortran have been used to validate the offloading concept.

Applications

The application developers, with the help of the support team from Task 8.7 through regular teleconference meetings, have progressed in their port to Intel\textsuperscript{\textregistered} Xeon Phi\textsuperscript{TM} using the MIC evaluator. Some of the developers have also started to hybridise their codes including OpenMP or OmpSs directives. Application profiling, debugging and optimisation have continued. Following the recommendations from last review, the project has made efforts to obtain access to larger Intel Xeon\textsuperscript{\textregistered} Phi\textsuperscript{TM} based systems. Accounts on Stampeded have been setup for all members of the support team and application developers that requested it. The remaining developers will obtain an account as soon as their applications are able to properly on the MIC evaluator, to avoid wasting the limited computing time available on Stampede. Access to two Intel Xeon\textsuperscript{\textregistered} Phi\textsuperscript{TM} clusters owned by Intel has been confirmed. The use of these systems is on a reservation basis.

\(^{1}\)To ease the reading, along the rest of the document the name KNC is used to designate Intel Xeon\textsuperscript{\textregistered} Phi\textsuperscript{TM}.
1.3 Expected final results

The DEEP project will have installed the DEEP System in Juelich (Germany), composed of two parts, the Cluster and the Booster, running with a software stack that allows applications to distribute their code on both parts of the machine, dynamically assigning Cluster Nodes to Booster Nodes and vice versa. The experience gained running six scientific applications on the DEEP System, with different code structures, requirements, and scientific goals, will demonstrate whether the proposed DEEP concept is suitable for the next generation Exascale supercomputers.
A.1 Listing of dissemination activities

This list reflects the disseminations activities performed between months 13 and 18 of the DEEP project.

Conferences, workshops, and meetings:

- **“Advanced Computer Architecture”** at Technical University Munich, Germany, January 30, 2013:
  - M.Ott (BADW-LRZ): “DEEP: Dynamical Exascale Entry Platform” (presentation)

- **2nd IS-ENES Workshop on “High performance computing for climate models”**, Fondation Bemberg, Toulouse, France, January 30 to February 1, 2013:
  - E.Suarez (JUELICH): “DEEP: Dynamical Exascale Entry Platform” (presentation)

- **Joint DEEP/Mont-Blanc internal Workshop**, Barcelona, Spain, March 14, 2013:
  - E.Suarez (JUELICH): “DEEP: Overview” (presentation)
  - H.Ch.Hoppe (Intel): “DEEP Architecture” (presentation)
  - Th.Moschny (ParTec): “DEEP Programming Model” (presentation)
  - J.Labarta (BSC): “OmpSs in DEEP and Mont-Blanc (presentation)
  - D.Alvarez (JUELICH): “DEEP Applications” (presentation)

- **HPC Advisory Council Switzerland Conference 2013**, Lugano, Switzerland, March 13-15, 2013:

- **Workshop on Strategic Development of High Performance Computers**, Tsukuba, Japan, March 18-19, 2013
  - N.Eicker (JUELICH): “The DEEP project” (presentation)

- **6th MEGWARE HPC User Meeting**, Chemnitz, Germany, April 25, 2013
  - N.Eicker (JUELICH): “The DEEP project” (presentation)

- **Exascale Applications and Software Conference**, Edinburgh, Scotland, UK. 9-11 April 2013:
  - G. Lapenta (KULeuven), et al. “Space Weather Applications for Exascale Computing” (presentation)
  - D.Alvarez (JUELICH), N.Eicker, E.Suarez and W.Guerich (JUELICH). “Programming model and application porting to the Dynamical Exascale Entry Platform (DEEP)” (presentation)

Publications, proceedings, press-releases, and newsletters:

- **EuroMPI 2013**, Madrid, Spain, September, 15-18, 2013:
  - S.Rinke (GRS), S.Prabhakaran (GRS), F.Wolf (GRS): “Efficient Offloading of Parallel Kernels Using MPI_Comm_Spawn” (submitted)
• HUCAA’13 (International Workshop on Heterogeneous and Unconventional Cluster Architectures and Applications), Lyon, France, October 1, 2013:
  o N.Eicker (JUELICH), Th.Lippert (JUELICH), Th.Moschny (ParTec), and E.Suarez (JUELICH): “The DEEP project: Pursuing cluster-computing in the many-core era” (submitted)

• Supercomputing Conference SC13, Denver, USA, November 18-21, 2013:
  o A.Galonska (JUELICH), N.Eicker (JUELICH), M.Nuessle (UniHD), J.Hauke (ParTec): “Bridging The DEEP Gap - Implementation of an Efficient Forwarding Protocol” (submitted)

  o D. Alvarez Mallon (JUELICH), N. Eicker (JUELICH), M.E. Innocenti (KULeuven), G. Lapenta (KULeuven), Th. Lippert (JUELICH), and E. Suarez (JUELICH): “On the Scalability of the Cluster-Booster concept”
List of Acronyms and Abbreviations

A

ADI3 layer: MPICH Abstract Device Interface Version 3
API: Application Programming Interface
ASIC: Application Specific Integrated Circuit: Integrated circuit customised for a particular use
Aurora: The name of Eurotech’s cluster systems
AVBP: A parallel CFD code for reactive unsteady flow simulations on hybrid grids developed by partner CERFACS

B

BADW-LRZ: Leibniz-Rechenzentrum der Bayerischen Akademie der Wissenschaften, Computing Centre, Garching, Germany
BI: Booster Interface (functional entity)
BIC: Booster Interface Card: Interface card to connect the Booster to the Cluster InfiniBand network
BIC evaluator: A platform consisting of three x86-based nodes equipped with (i) an EXTOLL NIC, (ii) an InfiniBand HCA, (iii) both, EXTOLL NIC and InfiniBand HCA, developed and used only in the DEEP project
BLAS: Basic Linear Algebra Subprograms: Standard application programming interface to publish basic linear algebra libraries
BlueGene/Q: Supercomputing architecture developed by IBM, well known for its energy efficiency, massive parallelism, 5D torus network and wide vector units.
BN: Booster Node (functional entity)
BNC: Booster Node Card: A physical instantiation of the BN
BNC evaluator: Same as EXTOLL evaluator
BoF: Birds of a Feather Session: Informal meeting during a Conference where people can discuss about the topic of their common interest
Booster System: Hardware subsystem of DEEP comprising of BNC, BIC and Intra-Booster network
BoP: Board of Partners for the DEEP project
BSC: Barcelona Supercomputing Centre, Spain
BSCW: Basic Support for Cooperative Work: Software package developed by the Fraunhofer Society, used to create a collaborative workspace for collaboration over the web

C

CERFACS: Centre Européen de Recherche et de Formation Avancée en Calcul Scientifique, Toulouse, France
CFD: Computational Fluid Dynamics
CG: Conjugate Gradient
CGGVS: CGGVeritas Services SA, Paris, France
CINECA: Consorzio Interuniversitario, Bologna, Italy
CN: Cluster Node (functional entity)
CooLMUC: Prototype at BADW-LRZ with direct warm water cooling
Coordinator: The contractual partner of the European Commission (EC) in the project
CPU: Central Processing Unit
CRESTA: Collaborative Research into Exascale Systemware, Tools & Applications: EU-FP7 Exascale Project led by the University of Edinburgh.
CUDA: Compute Unified Device Architecture: Parallel computing architecture developed by NVIDIA
CYI: Cyprus Institute, Nicosia, Cyprus

D
DC: Direct Current (electricity)
DDG: Design and Developer Group of the DEEP project
DEEP: Dynamical Exascale Entry Platform: EU-FP7 Exascale Project led by Forschungszentrum Juelich
DEEP Architecture: Functional architecture of DEEP (e.g. concept of an integrated Cluster Booster Architecture)
DEEP Booster: Booster part of the DEEP System
DEEP Supercomputer: A future Exascale supercomputer based on the DEEP Architecture
DEEP System: The production machine based on the DEEP Architecture developed and installed by the DEEP project
DFF: Dense Form Factor
DGEMM: Double precision General Matrix Matrix multiplication
DGEMV: Matrix-vector multiplication
Dimemas: A performance analysis tool for message-passing programs developed at BSC
DMA: Direct Memory Access
DoW: Description of Work: Annex I of the Grant Agreement
DSL: Domain Specific Language

E
EC: European Commission
EESI: European Exascale Software Initiative (FP7)
EMAC: ECHAM/MESSy (Application coupling together the ECHAM model with the MESSy framework)
EMEA: Europe, the Middle East and Africa: Regional designation used for government, marketing and business purposes
Energy Efficiency evaluator: Platform used for the investigations of the energy-aware functionality of DEEP, used only in the DEEP project
EPFL: École Polytechnique Fédérale de Lausanne, Switzerland
EU: European Union
Eurotech: Eurotech S.p.A., Amaro, Italy
Exaflop: $10^{18}$ floating point operations per second
Exascale: Computer systems or applications, which are able to run with a performance above $10^{18}$ floating point operations per second
EXTOLL: High speed interconnect technology for cluster computers developed by University of Heidelberg
EXTOLL evaluator: Platform for evaluation of EXTOLL technology, developed and used in the DEEP project
F
FLOP: Floating point Operation
FPGA: Field-Programmable Gate Array: Integrated circuit to be configured by the customer or designer after manufacturing

G
Global MPI: MPI allowing communication between the Booster and Cluster part of the DEEP System. Based on the ParaStation process-management and the Cluster-Booster protocol acting as a plug-in for the pscom library. Provides the MPI_Comm_spawn() call used by application processes running on the CNs to start additional processes on the BNs
GPU: Graphics Processing Unit
GRS: German Research School for Simulation Sciences GmbH, Aachen and Juelich, Germany

H
H4H: Hybrid programming For Heterogeneous architectures (EU project)
HCA: Host Channel Adapter
HOPSA: HOlistic Performance System Analysis (EU-Russia FP7 project)
HPC: High Performance Computing
HW: Hardware

I
IB: InfiniBand
ICPP: International Conference on Parallel Processing: Yearly conference on parallel and distributed computing
ICT: Information and Communication Technologies
IEEE: Institute of Electrical and Electronics Engineers
INFSO: Information Society
Intel: Intel GmbH, Feldkirchen, Germany
Intel Xeon® Phi™: official product name of the Intel Many Core (MIC) architecture processors. The first available Intel Xeon® Phi™ product is code-named Knights Corner (KNC).
Interconnect evaluator: Hardware for interconnect studies on physical and mechanical layer, developed and used in the DEEP project
I/O: Input/Output
IP: Intellectual Property or Internet Protocol (depending on the context)
iPIC3D: Programming code developed by the University of Leuven to simulate space weather
ISC: International Supercomputing Conference: Yearly conference on supercomputing which has been held in Europe since 1986

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DEEP - 287530 24.02.2014
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**JSC:** Juelich Supercomputing Center  
**JUDGE:** Juelich Dedicated GPU Environment: A cluster at the Juelich Supercomputing Centre  
**JUELICH:** Forschungszentrum Jülich GmbH, Jülich, Germany  
**JUQUEEN:** Juelich’s BlueGene/Q machine: A supercomputer installed at the Juelich Supercomputing Centre

**K**
- **KNC:** Knights Corner: Code name of a processor based on the MIC architecture. The commercial name of this product is Intel Xeon® Phi™.  
- **KNF:** Knights Ferry: Intel first available processor based on the MIC  
- **KULeuven:** Katholieke Universiteit Leuven, Belgium

**L**
- **LINPACK:** Software library to perform numerical linear algebra calculations used as benchmark  
- **LINUX:** A Unix-like computer operating system assembled under the model of free and open source software development and distribution

**M**
- **Maui:** Job scheduler for use on clusters and supercomputers  
- **MB:** Mega Byte or Mother Board (depending on the context)  
- **MC:** Monte Carlo  
- **MECCA:** Module Efficiently Calculating the Chemistry of the Atmosphere  
- **Mercurium compiler:** OmpSs’ source-to-source compiler  
- **MLNX:** Mellanox Technologies, Ltd., Sunnyvale, California and Yokneam, Israel  
- **MIC:** Intel Many Integrated Core architecture  
- **MIC evaluator:** Platform for evaluation of the MIC architectural concept, used only in the DEEP project  
- **MIC-OS:** Operating System of the MIC architecture  
- **Mini Booster prototype:** Minimal instantiation of a DEEP Booster used for analysis of the energy-aware functionality, developed and used in the DEEP project  
- **Mini DEEP System:** A fully featured DEEP System of minimal size comprising the Mini Booster  
- **MKL:** Intel® Math Kernel Library  
- **Mont-Blanc:** European scalable and power efficient HPC platform based on low-power embedded technology: EU-FP7 Exascale Project led by the Barcelona Supercomputing Centre  
- **MPI:** Message Passing Interface: API specification typically used in parallel programs that allows processes to communicate with one another by sending and receiving messages  
- **MPICH:** Freely available, portable implementation of MPI  
- **MQTT protocol:** Message Queue Telemetry Transport. Open message protocol for machine to machine communications. It enables the transfer of telemetry-style
data in the form of messages from pervasive devices, along high latency or constrained networks, to a server or small message broker.

**N**

NIC: Network Interface Card: Hardware component that connects a computer to a computer network

**O**

OmpSs: BSC’s Superscalar (Ss) for OpenMP
OpenCL: Open Computing Language to program GPUs
OpenMP: Open Multi-Processing: Application programming interface that support multiplatform shared memory multiprocesssing
OS: Operating System

**P**

ParaStation Consortium: Involved in research and development of solutions for high performance computing, especially for cluster computing
ParaStationMPI: Software for cluster management and control developed by ParTec
Paraver: Performance analysis tool developed by BSC
ParTec: ParTec Cluster Competence Center GmbH, Munich, Germany
PC: Normally Personal Computer, but in the context of the proposal also Project Coordinator
PCI: Peripheral Component Interconnect: Computer bus for attaching hardware devices in a computer
PCIe: PCI Express: Standard for peripheral interconnect, developed to replace the old standards PCI, improving their performance
PFlop/s: Petaflop, $10^{15}$ floating point operations per second
PIC: Particle In Cell
PM: Person Month or Project Manager of the DEEP project (depending on the context)
PMT: Project Management Team of the DEEP project
PR: Public Relations
PRACE: Partnership for Advanced Computing in Europe (EU project, European HPC infrastructure)
PRACE-1IP: PRACE First Implementation Phase (EU project)
Project Coordinator: Leading scientist coordinating and representing the DEEP project
Proto-Booster: Minimal instantiation of a DEEP Booster based on early access technologies (EXTOLL FPGA and KNC in PCIe form factor). Developed and used in the DEEP project for software development
PROSPECT: Promotion of Supercomputing Partnerships for European Competitiveness and Technology (registered association, Germany)
PUE: Power Usage Effectiveness

**Q**
QDR: Quad Data Rate: Communication signalling technique of InfiniBand

R
- RAS: Reliability, Availability and Serviceability
- RDMA: Remote Direct Memory Access
- RML: Risk management list used in the DEEP project
- RTD: Research and Technological Development
- RTM: Reverse Time Migration

S
- SC: International Conference for High Performance Computing, Networking, Storage, and Analysis, organised in the USA by the Association for Computing Machinery (ACM) and the IEEE Computer Society
- SCIF: Symmetric Communication Interface from Intel
- Scalasca: Performance analysis tool developed by JUELICH and GRS
- SIMD: Single Instruction, Multiple Data. Describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously
- SMFU: Shared Memory Functional Unit
- SRMIP: Soubaras-Remez Migration Parallel. Simulation code for seismic imaging used at partner CGGVS
- StarSs: Generic programming environment developed by BSC
- Stampede: Supercomputer (Dell PowerEdge C8220 Cluster with Intel Xeon Phi coprocessors) installed at Texas Advanced Computing Center from Univ. of Texas, in the USA. It is nr. 7 in the TOP500 list today
- STRATOS: PRACE advisory group to foster development of HPC technologies in Europe
- SW: Software

T
- TCO: Total Cost of Ownership
- TFlop/s: Teraflop, $10^{12}$ floating point operations per second
- Tier-0, Tier-1, …: Different classes of supercomputers ordered by their performance
- TIM: Thermal Interface Material
- TK: Task, followed by a number: Term to designate a task inside a work package of the DEEP project
- Torque: Distributed resource manager providing control over batch jobs and distributed compute nodes
- ToW: Team of Work Package leaders within the DEEP project
- TP10: Third Party under Clause 10
- TurboRVB: Quantum Monte Carlo Software for electronic structure calculations, developed by SISSA

U
- UniHD: University of Heidelberg, Germany
UniReg: University of Regensburg, Germany

VELO: Virtualised Engine for Low Overhead: An EXTOLL communications channel

WP: Work Package

x86: Family of instruction set architectures based on the Intel 8086 CPU