DEEP

Dynamical Exascale Entry Platform

Grant Agreement Number: 287530

D1.3
Periodic progress report at month 12

Approved

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## Project and Deliverable Information Sheet

<table>
<thead>
<tr>
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</tbody>
</table>

* - The dissemination level are indicated as follows: PU – Public, PP – Restricted to other participants (including the Commission Services), RE – Restricted to a group specified by the consortium (including the Commission Services). CO – Confidential, only for members of the consortium (including the Commission Services).

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<table>
<thead>
<tr>
<th>Document</th>
<th>Title: Periodic progress report at month 12</th>
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</thead>
<tbody>
<tr>
<td>ID:</td>
<td>D1.3</td>
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</tbody>
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<tr>
<th>Authorship</th>
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<tbody>
<tr>
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<td>V.Beltran (BSC), D.Alvarez (JUELICH), A.Auweter (BADW-LRZ), N.Eicker (JUELICH), J.Kreutz (JUELICH), L.Palm (BADW-LRZ), H.Ch.Hoppe (Intel), N.Eicker (JUELICH)</td>
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<tr>
<td>Approved by:</td>
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</tbody>
</table>
### Document Status Sheet

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Status</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
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</tr>
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</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Keywords</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

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Executive Summary

The Dynamical Exascale Entry Platform (DEEP) project started on 1st December 2011 and will last three years. The main goal of the project is to develop a prototype hardware and software supercomputing system with the potential to reach a peak performance of 100 PFlop/s in 2014, paving the way towards Exascale systems by the end of the decade. DEEP will optimise a set of grand-challenge applications with high societal impact and generic algorithmic structure for this platform. The key innovation of the DEEP project is its holistic Exascale-enabling concept integrating the architectural, system software and application level. The strategic goals of DEEP are (i) to contribute to an independent provision of general purpose Exascale performance supercomputers for the European HPC research infrastructure PRACE, (ii) to advance the growth of ICT and HPC hardware and software technology developed and produced in Europe, and (iii) to expand worldwide leadership and competitiveness of Europe’s computational scientists and engineers.

This report describes the objectives, work performed, resources used, and results achieved during months 7 to 12 of the DEEP project. The main achievements in the reporting period are enumerated below:

- First review (at month 6) successfully passed.
- Environment at Juelich prepared for the installation of the DEEP System.
- Installation of the DEEP Cluster and auxiliary servers at Juelich.
- Define the concepts to be applied in DEEP for improving energy and cooling efficiency of computing systems.
- Progress in the DEEP Booster design: backplane design finished; preliminary BNC design based on PCIe form factor and EXTOLL FPGA ready.
- Implementation of the first complete version of low-level Cluster-Booster protocol.
- First prototype of the programming environment for BN ready.
- Identification of the optimal distribution of the applications code between Cluster and Booster.
- Presentation of DEEP in publications, workshops and conferences, the most important of them the ISC’12 in Hamburg and the SC12 in Salt Lake City.
- Participation (together with Mont-Blanc) on a training workshop on OmpSs for application developers.
1 Publishable summary

Numerous challenges must be overcome to reach Exascale by the end of the decade. When starting from current PFlop systems a factor of 1000 in performance increase is required. Investigating the roadmaps of standard CPUs reveals that it will not be sufficient to update and scale the concept of current cluster systems. In order to meet the requirements of energy-efficiency the use of accelerators becomes inevitable. However, today's solution of accelerated clusters – i.e. cluster with accelerators attached to each node – will not carry us to Exascale. On the one hand this is due to the inflexibility originating from the static assignment of standard CPUs and accelerators; on the other hand the competing use of the system bus by both accelerator and interconnect, combined with the lack of ability of the accelerator to use the interconnect autonomously, limits the scalability of this solution seriously.

Therefore, the DEEP Architecture proposes to detach the accelerators from the standard CPUs and to gather them into a separate cluster of accelerators that is called Booster. It is foreseen to run the highly scalable parts of the applications on this part of the DEEP System. The Booster is connected to a standard Cluster qualified to handle those parts of an application not suited for the Booster. The benefits are manifold: there is more flexibility on the ratio of standard CPUs and accelerators to be used by an application, the ability of the accelerators in the Booster to act autonomously allows for off-loading more complex and more parallel kernels, and an extended programming-model will support the application-developers in the identification of these offload-kernels and in porting their workload to the proposed architecture.

1.1 Project objectives

The specific objectives of the DEEP project are:

- Development of a prototype hardware platform consisting of a Cluster element based on multi-core-chips, a Booster element based on many-core technology and a commensurate connectivity, following the components-off-the-shelf philosophy. This prototype of Cluster Booster Architecture will serve as proof-of-concept for a next-generation PRACE production system reaching up to 100 PFlop/s in the time-frame 2014/2015, with the potential to achieve Exascale between 2018 and 2020.
  - Cluster part is already installed at JUELICH.
  - Prototypes of several Booster components are being tested
- Combination of innovative technologies for the Booster element: novel Intel many-core processors, EXTOLL high speed interconnect, hot water cooling.
  - First prototypes of Booster Node Card (BNC) are already available. One BNC contains two nodes, each with an Intel Xeon\textsuperscript{®} Phi\textsuperscript{TM} and an EXTOLL FPGA to implement the network.
- Development of a reliable, open source cluster operating system, interconnect and runtime software stack with high resilience while exploiting millions of cores.
  - Software environment and programming model for DEEP have been defined.
  - First implementation of the Cluster Booster low level protocol is available. Its description is given in Deliverable D4.2.
OmpSs runtime (Nanos++) is already ported to Intel Xeon® Phi™. Details are given in D5.1.

- Development of programming models, scientific libraries and performance tools for standard x86-based many-core processors, in order to achieve high productivity and enabling unprecedented scalability.
  - First performance measurements of Intel MKL BLAS library routines have taken place. Results are described in D5.1.

- Improvement of current cluster energy efficiency by an order of magnitude exploiting novel many-core chip technologies and advanced software-aided cooling technologies with a power usage effectiveness approaching a value of 1.
  - Hot water cooling infrastructure has been prepared in JUELICH (D6.2).
  - Concepts for improving energy and cooling efficiency are discussed in D7.2.

- Optimisation of a set of application codes on the DEEP System that are representative for future Exascale computing and data handling requirements, chosen from the fields of Health and Biology, Climatology, Seismic Imaging, Computational Engineering, Space Weather, and Superconductivity and proving safe extrapolation to millions of cores as will be required with future Exascale systems.
  - The structure of the applications has been analysed and initial strategies to distribute the codes between Cluster and Booster has been identified (see D8.1).

- Demonstration of scalability of the new hardware-software concept with respect to the generic multi-scale, adaptive grid and long-range force parallelisation models underlying the application codes.
  - Demonstration will be first possible when the complete system is available.

- Dissemination of the innovations and results of the project to the public.
  - The DEEP project and its first results have been presented in multiple meeting, conferences, and workshops. Details are given in D2.3. Also, a list of dissemination activities is provided in Annex A.1 of the present report.

### 1.2 Work performed and main results

During the months 7 to 12 the DEEP project has achieved two of the three milestones that were set for this reporting period:

- the definition of concepts for improving energy efficiency of the Booster
- the preparation of the environment for the DEEP System at JUELICH.

The successful completion of the second project review will be the third milestone. All deliverables have been submitted in time and the review itself is scheduled for January 18th, 2013. The project is ahead of time in the installation of the DEEP Cluster subsystem, which is almost complete. The only step missing to achieve Milestone number 17, due in month 16, is the connection of the InfiniBand® network, planned for Q1-2013.

**Management, legal and administrative tasks**

In this reporting period the DEEP project is already in a phase of regular operation, where the management activities focus on monitoring the progress of the project to guarantee the
achievement of all technical goals specified in the Description of Work (DoW) and the fulfillment of all commitments to the European Commission.

The Management team had organised the agenda for the first review meeting (at month 6) which took place on the 12th June 2012 in Brussels. To fulfil the internal quality policies a rehearsal meeting one day before the review was conducted. As a result of the first review, it was stated “the project has fully achieved its objectives and technical goals for the period and has even exceeded expectations”. Additionally, all deliverables submitted in the first six months of the project were approved. The comments from the reviewers and their recommendations concerning future work are addressed in section Error! Reference source not found.

Monthly teleconferences of the Team of Work Package leaders (ToW) were organised to periodically discuss the progress in all Work Packages (WPs). The third regular face-to-face meeting of the consortium (BoP) took place in Leuven (Belgium) on the 23rd – 24th October 2012. Here the status of the project was discussed, with particular emphasis on the content of the eight Deliverables that had to be submitted by end of November 2012, and on the preparation for the upcoming review at month 12. All Deliverables were timely submitted to the European Commission after having passed through the mandatory DEEP internal review process.

In the time period there has not been any change in the legal framework established by the Grant Agreement and the Consortium Agreement.

**Dissemination, training and outreach**

The centre of the dissemination activities of DEEP is its web site: www.deep-project.eu. The DEEP web page has been updated in the reporting period to keep track with the project results, for instance with the evolution of the DEEP SW stack. Updates were made to inform on news, upcoming events and job vacancies, and to make DEEP’s public material available, including the approved public Deliverables.

The slides presented in open Workshops and Conferences are also published on the DEEP website.

Partners from the DEEP consortium presented the project’s concept in several conferences and workshops, including the two most important events in the HPC community: the International Supercomputing Conference (ISC’12) and the Supercomputing Conference (SC12) that took place in Europe and the USA, respectively. At a satellite session “The European Way to Exascale” during ISC’12 the three European Exascale projects CRESTA, DEEP, and Mont-Blanc were presented to an audience of about 75 people. During SC12 the BoF (Birds of a Feather) session “Exascale Research – The European Approach” the three projects highlighted their objectives and results to an international audience. A flyer explaining the goals and most important aspects of the DEEP project was distributed at ISC’12 and an updated version was produced and handed out at SC12. Two completed boards of the Booster Node evaluator were shown at SC12 at the booths of partners JUELICH and Eurotech.

Training the community on how to use the software and hardware developed in DEEP is an important part of the project. The main goal of the training events in DEEP is to teach the application developers participating in the project on how to use the software tools and programming environment running on the DEEP System and other intermediate prototypes. The second DEEP Training Workshop took place from the 8th to the 10th October 2012 in Barcelona (Spain). An intensive course including lectures and numerous hands-on sessions on
the OmpSs programming environment (BSC), with special focus on its support for Fortran, was offered to all members of the DEEP and Mont-Blanc projects.

All dissemination and training activities performed in the present reporting period are described in Deliverable D2.3.

**Technical Work**

The technical work in DEEP is grouped into the three main parts: system hardware, system software, and applications.

In the hardware concept of DEEP (see Figure 1) a standard Cluster, composed of multi-core processors and the high flexibility network InfiniBand®, is attached to a Booster of Intel Xeon® Phi™ processors connected via a highly scalable EXTOLL torus network. The DEEP software stack (see Figure 3) focuses on scalability and an efficient use of resources. The parts of the application with a complex communication pattern (low to medium scalability) will run on the DEEP Cluster, while the code parts with regular communication patterns (highly scalable) will run on the Booster. The DEEP programming environment provides a Global MPI layer below the OmpSs (BSC) tasking model to help the developers in decomposing their applications into tasks in order to efficiently overlap the use of the Cluster and the Booster sides.

![Figure 1: Sketch of DEEP hardware architecture (CN: Cluster Node; BN: Booster Node; BI: Booster Interface)](image)

**System Hardware**

On the hardware side the work within the reporting period has progressed in the design of the various elements of the DEEP Booster. The design of the Booster Node Card (BNC) first version, based on a standard PCI Express form factor Intel® Xeon Phi™ and an Altera Stratix V FPGA running EXTOLL, is finished and the first BNC boards have come back from the factory (see Figure 2). These first samples will be used to finalise the mechanical and electric design of the final Booster chassis and for backplane functionality tests. The design of the Booster backplane is ready, and its production will start as soon as the functionality of the backplane prototype is verified.

The preparation of the infrastructure for the DEEP System did conclude in August 2012, and is described in detail in Deliverables D6.1 and D6.2. Additionally, Deliverable D7.2 describes the concepts implemented in DEEP to improve the energy and cooling efficiency of HPC computing systems.

In September 2012, one month ahead of schedule, the DEEP Cluster was installed at Juelich. Its 128 computing nodes, each containing two Intel® Xeon® E5 (code name “Sandy Bridge”)

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CPUs, were integrated into Eurotech’s Aurora rack and connected to power supply and water cooling. Functional tests performed for the acceptance of the system demonstrated the perfect functioning of all nodes and the capability of the water cooling system to dissipate all the waste heat generated during stress tests. A small LINPACK benchmark provided by Eurotech was executed locally on all nodes, and achieved about 90% peak performance on all nodes, which is a good result for the kind of non-optimised benchmark used for the tests. LINPACK will be tested across all nodes as soon as the InfiniBand® network is connected. This is expected to happen in Q1/2013 and will conclude the installation of the DEEP Cluster. The Cluster is already available to users, who can work with the system using the fully functioning Gigabit Ethernet network. The DEEP Cluster, its environment and the login and file system servers are part of the in-kind contribution to the project by JUELICH.

Figure 2: Photo of a BNC Evaluator Board.

System Software

On the software side, the implementation and porting of the various elements involved in the DEEP software stack has progressed in the present reporting period according to plan. The lowest layer of the software environment, the Cluster-Booster protocol, has already been defined and its first implementation is finished. Its characteristics are detailed in Deliverable D4.2. The first prototype of the DEEP programming environment in a Booster Node has been produced and is described in Deliverable D5.1.

Following the meetings and discussions between system software and application developers in the last 6 months, the diagram of the software stack provided in the DoW was updated (see Figure 3). It was found that the MPI-2 standard provides an API fulfilling all the requirements needed for application offload from the Cluster to the Booster. This induced the foundation of a working group for the design of a Global MPI layer. This group, constituted by members of GRS, JUELICH, and its Third Party Partner ParTec, meets face-to-face in a monthly basis. In this frame, the tasks required to provide Global MPI have been identified and distributed between the members of the working group. Their implementation has started.

The hardware evaluators built in the first months of the project have been used in the present reporting period as platforms for software implementation.
• **MIC evaluator**: in addition to the existing three standard server machines containing one KNF software development vehicle each, two new servers containing Intel Xeon® Phi™ cards are now installed at JUELICH. The performance of basic BLAS libraries has been measured on these systems to compare the results with those obtained on standard Intel® Xeon® processors.

• **EXTOLL evaluator**: based on commodity hardware connecting multiple KNF software development vehicles through EXTOLL. Used for starting the port of EXTOLL driver to the Intel® Xeon Phi™ OS.

• **Interconnect evaluator part1**: a board assembled at UniHD with one EXTOLL FPGA and one KNF software development vehicle to make tests of the communication between EXTOLL and KNF. This evaluator serves to explore the ability of the EXTOLL network to boot MIC cards.

• **Interconnect evaluator part2 (BNC evaluator)**: board containing one KNF software development vehicle and one EXTOLL FPGA assembled at Eurotech to test signal integrity, mechanical and thermal issues. Both this evaluator and the previous one are described in detail in Deliverable D3.2.

• **BIC evaluator**: system installed at UniHD and constituted by three PCs, one with InfiniBand, one with EXTOLL, and one with both. This is the platform used to develop Cluster-Booster protocol.

![Diagram of the updated DEEP software architecture](image)

**Figure 3: Diagram of the updated DEEP software architecture**

**Applications**

The application developers, with the help of the support team from Task 8.7 through face-to-face hand-on sessions in Barcelona and Juelich, have analysed in detail the structure of the DEEP applications. The result of these analyses is the first approach on how to divide the applications between Cluster and Booster. The parts identified as highly scalable, and therefore in principle suitable for the DEEP Booster, have been tested on JUQUEEN, a BlueGene/Q system from JUELICH. The CPU time was provided to the project as in-kind contribution. The goal of these tests is to verify the high scalability of the selected code parts in a system with a topology and characteristics similar to the DEEP Booster. The results of those measurements and experiments are detailed in Deliverable D8.1.
1.3 Expected final results

The DEEP project, at the end of its three years duration, will have installed the DEEP System in Juelich (Germany), composed of two parts, the Cluster and the Booster, running with a software stack that allows applications to distribute their code on both parts of the machine, dynamically assigning Cluster Nodes to Booster Nodes and vice versa. The experience gained running six scientific applications on the DEEP System, with different code structures, requirements, and scientific goals, will demonstrate whether the proposed DEEP concept is suitable for the next generation Exascale supercomputers.
Annex A

A.1 Listing of dissemination activities

This list reflects the disseminations activities performed between months 7 and 12 of the DEEP project.

Conferences, workshops, and meetings:

- **EU-Russia APOS/HOPSA Workshop**, Moscow, Russia, May 30, 2012
  - B. Mohr (JUELICH): “The DEEP Project” (presentation)

- **ISC’12**, Hamburg, Germany, June 18-21, 2012
  - Th. Lippert (JUELICH), June 20, 2012 (presentation at Intel’s Booth)
  - H. Ch. Hoppe (Intel), G. Lapenta (KULeuven), F. Delalandre (EPFL), N. Eicker (JUELICH), and E. Suarez (JUELICH) (DEEP demo station at the Intel booth with focus on architecture and two applications)

  - N. Eicker (JUELICH), “On the Scalability of the Cluster-Booster concept” (presentation)

- **HPC 2012 Workshop**, Cetaro, Italy, June 27, 2012

- **Junior Chamber International (JCI) European Conference**, Braunschweig, Germany, June, 13-17, 2012
  - M. Kauschke and M. Richter (Intel), “The DEEP project” (presentation and MIC demo)

- **ScalPerf 2012**, University Residential Center Bertinoro (Forlì-Cesena), Italy, September 23-27, 2012:
  - G. Tecchiolli (Eurotech): "System-level Energy-efficient scalable HPC" (presentation)

- **Research @ Intel Europe**, Princesa Sofia Hotel, Barcelona, Spain, October 22-23, 2012:
  - J. Labarta (BSC), “The OmpSs Model on Intel® Xeon Phi™”, presentation and demo
• **Supercomputing Conference 2012**, Salt Lake City, Utah, USA, November 12-15, 2012
  - E. Suarez (JUELICH): “DEEP” (Theater presentation at the Intel’s Booth, November 14, 2012)
  - H.Ch. Hoppe (Intel), G. Lapenta (KULeuven) (demo at the JSC booth with focus on showing the Space Weather Application running on an Intel Xeon® PhiTM card)
  - L. Palm (BADW-LRZ), distribution of DEEP flyers and stickers at partners’ Booths.

  - V.Beltran (BSC), "Programming Challenges of the DEEP Architecture" (presentation)

Publications, proceedings, press-releases, and newsletters:

  - D. Alvarez Mallon (JUELICH), N. Eicker (JUELICH), M.E. Innocenti (KULeuven), G. Lapenta(KULeuven), Th. Lippert (JUELICH), and E. Suarez (JUELICH): “On the Scalability of the Cluster-Booster concept”

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  - H. Huber and A.Auweter (BADW-LRZ): „Exascale Computing: Energieeffizienz für die Supercomputer von morgen“ (Article in German)

  - P.Arts (Eurotech): “Eurotech delivers hot water cooled HPC to Jülich”.

  - E.Suarez (JUELICH): “DEEP: Boosting computing towards Exascale”.

  - Th. Lippert, N. Eicker, E. Suarez (all JUELICH): “A Shining Star Lights Up the Road to Exascale” (Interview written by reporter Mike Bernhardt)
List of Acronyms and Abbreviations

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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit: Integrated circuit customised for a particular use</td>
</tr>
<tr>
<td>Aurora</td>
<td>The name of Eurotech’s cluster systems</td>
</tr>
</tbody>
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<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>BADW-LRZ</td>
<td>Leibniz-Rechenzentrum der Bayerischen Akademie der Wissenschaften. Computing Centre, Garching, Germany</td>
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<tr>
<td>BI</td>
<td>Booster Interface (functional entity)</td>
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<td>BIC</td>
<td>Booster Interface Card: Interface card to connect the Booster to the Cluster InfiniBand network</td>
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<td>BIC evaluator</td>
<td>A platform consisting of three x86-based nodes equipped with (i) an EXTOLL NIC, (ii) an InfiniBand HCA, (iii) both, EXTOLL NIC and InfiniBand HCA, developed and used only in the DEEP project</td>
</tr>
<tr>
<td>BLAS</td>
<td>Basic Linear Algebra Subprograms: Standard application programming interface to publish basic linear algebra libraries</td>
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<tr>
<td>BlueGene/Q</td>
<td>Supercomputing architecture developed by IBM, well known for its energy efficiency, massive parallelism, 5D torus network and wide vector units.</td>
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<tr>
<td>BN</td>
<td>Booster Node (functional entity)</td>
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<tr>
<td>BNC</td>
<td>Booster Node Card: A physical instantiation of the BN</td>
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<tr>
<td>BNC evaluator</td>
<td>Same as EXTOLL evaluator</td>
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<tr>
<td>BoF</td>
<td>Birds of a Feather Session: Informal meeting during a Conference where people can discuss about the topic of their common interest</td>
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<td>Booster System</td>
<td>Hardware subsystem of DEEP comprising of BNC, BIC and Intra-Booster network</td>
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<td>BoP</td>
<td>Board of Partners for the DEEP project</td>
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<td>BSC</td>
<td>Barcelona Supercomputing Centre, Spain</td>
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<tr>
<td>BSCW</td>
<td>Basic Support for Cooperative Work: Software package developed by the Fraunhofer Society, used to create a collaborative workspace for collaboration over the web</td>
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</tbody>
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<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>CERFACS</td>
<td>Centre Européen de Recherche et de Formation Avancée en Calcul Scientifique, Toulouse, France</td>
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<tr>
<td>CFD</td>
<td>Computational Fluid Dynamics</td>
</tr>
<tr>
<td>CGGVS</td>
<td>CGGVeritas Services SA, Paris, France</td>
</tr>
<tr>
<td>CINECA</td>
<td>Consorzio Interuniversitario, Bologna, Italy</td>
</tr>
<tr>
<td>CN</td>
<td>Cluster Node (functional entity)</td>
</tr>
<tr>
<td>CooLMUC</td>
<td>Prototype at BADW-LRZ with direct warm water cooling</td>
</tr>
<tr>
<td>Coordinator</td>
<td>The contractual partner of the European Commission (EC) in the project</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
</tbody>
</table>
| CRESTA | Collaborative Research into Exascale Systemware, Tools & Applications: EU-FP7 Exascale Project led by the University of Edinburgh.
**CUDA:** Compute Unified Device Architecture: Parallel computing architecture developed by NVIDIA

**CYI:** Cyprus Institute, Nicosia, Cyprus

**D**

**DC:** Direct Current (electricity)

**DDG:** Design and Developer Group of the DEEP project

**DEEP:** Dynamical Exascale Entry Platform: EU-FP7 Exascale Project led by Forschungszentrum Juelich

**DEEP Architecture:** Functional architecture of DEEP (e.g. concept of an integrated Cluster Booster Architecture)

**DEEP Booster:** Booster part of the DEEP System

**DEEP Supercomputer:** A future Exascale supercomputer based on the DEEP Architecture

**DEEP System:** The production machine based on the DEEP Architecture developed and installed by the DEEP project

**DFF:** Dense Form Factor

**DMA:** Direct Memory Access

**DoW:** Description of Work: Annex I of the Grant Agreement

**E**

**EC:** European Commission

**EESI:** European Exascale Software Initiative (FP7)

**EMEA:** Europe, the Middle East and Africa: Regional designation used for government, marketing and business purposes

**Energy Efficiency evaluator:** Platform used for the investigations of the energy-aware functionality of DEEP, used only in the DEEP project

**EPFL:** École Polytechnique Fédérale de Lausanne, Switzerland

**EU:** European Union

**Eurotech:** Eurotech S.p.A., Amaro, Italy

**Exaflop:** $10^{18}$ floating point operations per second

**Exascale:** Computer systems or applications, which are able to run with a performance above $10^{18}$ floating point operations per second

**EXTOLL:** High speed interconnect technology for cluster computers developed by University of Heidelberg

**EXTOLL evaluator:** Platform for evaluation of EXTOLL technology, developed and used in the DEEP project

**F**

**FLOP:** Floating point Operation

**FPGA:** Field-Programmable Gate Array: Integrated circuit to be configured by the customer or designer after manufacturing

**G**

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**Global MPI:** MPI allowing communication between the Booster and Cluster part of the DEEP System. Based on the ParaStation process-management and the Cluster-Booster protocol acting as a plug-in for the pscom library. Provides the MPI_Comm_spawn() call used by application processes running on the CNs to start additional processes on the BNs.

**GPU:** Graphics Processing Unit

**GRS:** German Research School for Simulation Sciences GmbH, Aachen and Juelich, Germany

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**H**

**H4H:** Hybrid programming For Heterogeneous architectures (EU project)

**HCA:** Host Channel Adapter

**HOPSA:** HOlistic Performance System Analysis (EU-Russia FP7 project)

**HPC:** High Performance Computing

**HW:** Hardware

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**I**

**IB:** InfiniBand

**ICPP:** International Conference on Parallel Processing: Yearly conference on parallel and distributed computing

**ICT:** Information and Communication Technologies

**IEEE:** Institute of Electrical and Electronics Engineers

**INFSO:** Information Society

**Intel:** Intel GmbH, Feldkirchen, Germany

**Intel Xeon® Phi™:** official product name of the Intel Many Core (MIC) architecture processors. The first available Intel Xeon® Phi™ product is code-named Knights Corner (KNC).

**Interconnect evaluator:** Hardware for interconnect studies on physical and mechanical layer, developed and used in the DEEP project

**I/O:** Input/Output

**IP:** Intellectual Property or Internet Protocol (depending on the context)

**ISC:** International Supercomputing Conference: Yearly conference on supercomputing which has been held in Europe since 1986

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**J**

**JSC:** Juelich Supercomputing Center

**JUDGE:** Juelich Dedicated GPU Environment: A cluster at the Juelich Supercomputing Centre

**JUELICH:** Forschungszentrum Jülich GmbH, Jülich, Germany

**JUQUEEN:** Juelich’s BlueGene/Q machine: A supercomputer installed at the Juelich Supercomputing Centre

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**K**

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KNC: Knights Corner: Code name of a processor based on the MIC architecture. The commercial name of this product is Intel Xeon® Phi™.

KNF: Knights Ferry: Intel first available processor based on the MIC

KULeuven: Katholieke Universiteit Leuven, Belgium

LINPACK: Software library to perform numerical linear algebra calculations used as benchmark

LINUX: A Unix-like computer operating system assembled under the model of free and open source software development and distribution

MB: Mega Byte or Mother Board (depending on the context)

MC: Monte Carlo

MLNX: Mellanox Technologies, Ltd., Sunnyvale, California and Yokneam, Israel

MIC: Intel Many Integrated Core architecture

MIC evaluator: Platform for evaluation of the MIC architectural concept, used only in the DEEP project

MIC-OS: Operating System of the MIC architecture

Mini Booster prototype: Minimal instantiation of a DEEP Booster used for analysis of the energy-aware functionality, developed and used in the DEEP project

Mini DEEP System: A fully featured DEEP System of minimal size comprising the Mini Booster

MKL: Intel® Math Kernel Library

Mont-Blanc: European scalable and power efficient HPC platform based on low-power embedded technology: EU-FP7 Exascale Project led by the Barcelona Supercomputing Centre

MPI: Message Passing Interface: API specification typically used in parallel programs that allows processes to communicate with one another by sending and receiving messages

MPICH: Freely available, portable implementation of MPI

NIC: Network Interface Card: Hardware component that connects a computer to a computer network

OmpSs: BSC’s Superscalar (Ss) for OpenMP

OpenCL: Open Computing Language to program GPUs

OpenMP: Open Multi-Processing: Application programming interface that support multiplatform shared memory multiprocessing

OS: Operating System

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ParaStation Consortium: Involved in research and development of solutions for high performance computing, especially for cluster computing
ParaStationMPI: Software for cluster management and control developed by ParTec
Paraver: Performance analysis tool developed by BSC
ParTec: ParTec Cluster Competence Center GmbH, Munich, Germany
PC: Normally Personal Computer, but in the context of the proposal also Project Coordinator
PCI: Peripheral Component Interconnect: Computer bus for attaching hardware devices in a computer
PCle: PCI Express: Standard for peripheral interconnect, developed to replace the old standards PCI, improving their performance
PFlop/s: Petaflop, $10^{15}$ floating point operations per second
PIC: Particle In Cell
PM: Person Month or Project Manager of the DEEP project (depending on the context)
PMT: Project Management Team of the DEEP project
PR: Public Relations
PRACE: Partnership for Advanced Computing in Europe (EU project, European HPC infrastructure)
PRACE-1IP: PRACE First Implementation Phase (EU project)
Project Coordinator: Leading scientist coordinating and representing the DEEP project
PROSPECT: Promotion of Supercomputing Partnerships for European Competitiveness and Technology (registered association, Germany)
PUE: Power Usage Effectiveness

Q
QDR: Quad Data Rate: Communication signalling technique of InfiniBand

R
RAS: Reliability, Availability and Serviceability
RDMA: Remote Direct Memory Access
RML: Risk management list used in the DEEP project
RTD: Research and Technological Development

S
SC: International Conference for High Performance Computing, Networking, Storage, and Analysis, organised in the USA by the Association for Computing Machinery (ACM) and the IEEE Computer Society
Scalasca: Performance analysis tool developed by JUELICH and GRS
SMFU: Shared Memory Functional Unit
StarSs: Generic programming environment developed by BSC
STRATOS: PRACE advisory group to foster development of HPC technologies in Europe
SW: Software
T
TCO: Total Cost of Ownership
TFlop/s: Teraflop, $10^{12}$ floating point operations per second
Tier-0, Tier-1, …: Different classes of supercomputers ordered by their performance
TK: Task, followed by a number: Term to designate a task inside a work package of the DEEP project
ToW: Team of Work Package leaders within the DEEP project

U
UniHD: University of Heidelberg, Germany
UniReg: University of Regensburg, Germany

V
VELO: Virtualised Engine for Low Overhead: An EXTOLL communications channel

W
WP: Work Package

X
x86: Family of instruction set architectures based on the Intel 8086 CPU

Y

Z